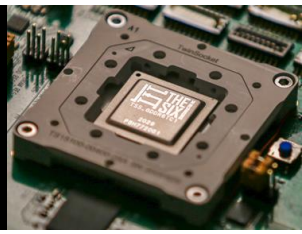
GDDR6 PHY
TSMC12FFc

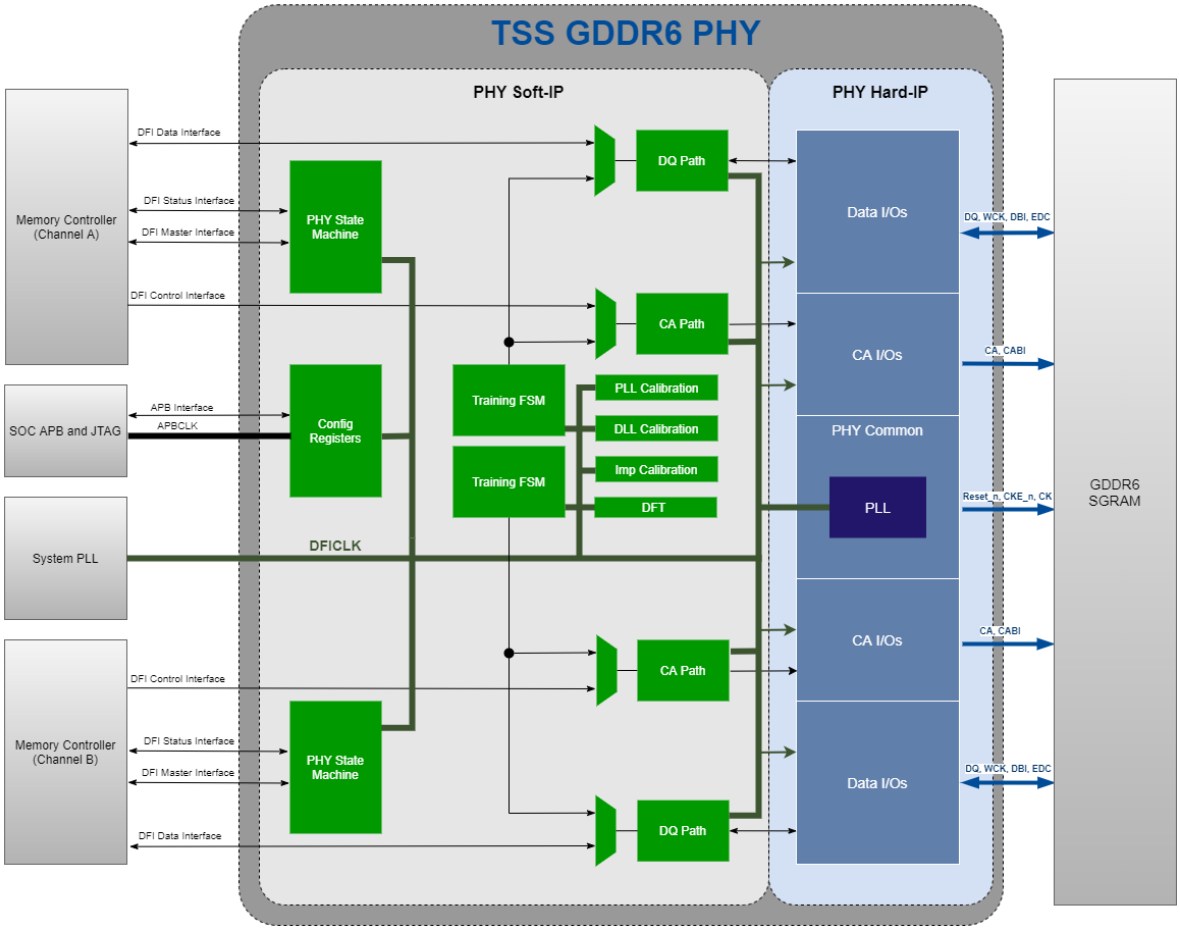


Overview

With the advancement of artificial intelligence (AI), deep neural networks (DNN), ADAS, and high-performance computing (HPC), there is an ever-increasing demand for higher memory bandwidth. Along with the large amount of data generated by these applications, the memory sub-system plays a crucial role in the overall performance.

TSS GDDR6 PHY utilizes state-of-the-art architecture in full custom analog mixed-signal design to overcome the problem of long-term impedance drift and clock phase drift, allowing impedance and clock phase updates without the need to interrupt data traffic. The programmable timing PHY boundary combines flexibility with analog precision. The result is ultra low PHY read/write latency between the memory controller and the GDDR6 DRAM without sacrificing performance.

At the system level, TSS GDDR6 PHY was designed with minimal package substrate layer and PCB layer count in mind. This enables the integration of a GDDR6 memory sub-system solution in sensitive applications, such as consumer edge devices, digital set-top-box and TV, SSD controllers, and application processors.



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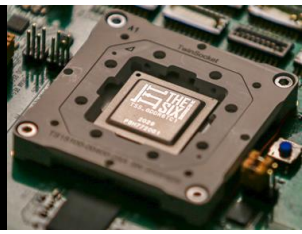

Key Features

DRAM supports
- *JEDEC JESD250 compliant GDDR6 support up to 16Gbps*
- *X16 mode, X8 mode, and pseudo-channel mode*
- *Low frequency RDQS mode support*

High Performance
- *Channel equalization with FFE, CTLE, and DFE*
- *Continuous IO impedance and timing phase updates with no traffic interruption*

DFT Features
- *IO internal/external loopback*
- *Integrated PRBS generator/checker*
- *IO bypass mode for internal clock observation*
- *Analog test ports for internal analog signals observation*

Special Features
- *PHY independent initialization of DRAM and training – no memory controller involved*

Benefits

Power Advantage
- *Supports multiple frequency states with fast switching time*
- *Multiple power saving states with various exit times*
- *Supports DFI frequency ratios of 1:2 and 1:4*

Ultra Low Latency
- *Ultra low read/write latency with programmable PHY boundary timing*

Low Implementation BOM Cost
- *Support low cost 2-2-2 package substrate*
- *Designed for 6-layer PCB as the minimum layer count*

Deliverables

- **PHY Databook**
- **Implementation Guideline**
- **Package and PCB Design Guideline**
- **Test and Characterization Guideline**

- **Hard-IP Layout (GDS II)**
- **Hard-IP Layout Abstract (LEF)**
- **Hard-IP Liberty Timing Models (.lib)**
- **Hard-IP LVS Netlist (CDL)**
- **IO IBIS models**

- **Verilog Behavior Models and RTL**
- **Example Test Benches**
- **Synthesis and STA Constraints**
- **Physical Verification Reports**