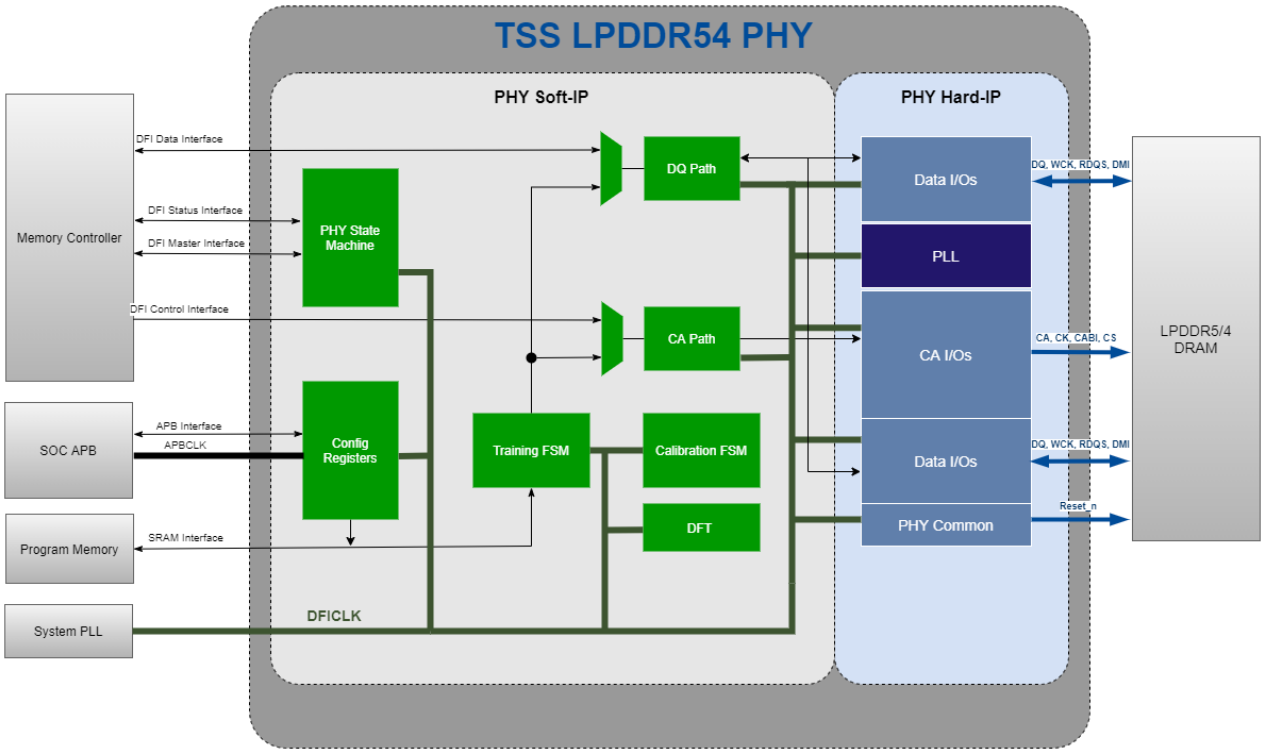
LPDDR54 PHY

Overview

Consumer mobile and edge devices are processing large amounts of data in today's applications, ranging from video processing, mobile gaming, to AI-based image recognition. As a result of these advancements, the memory sub-system plays a crucial role in the overall performance.

The TSS LPDDR54 PHY utilizes state-of-the-art architecture to maximize timing and voltage margins over process, voltage and temperature variations, while minimizing interruption to data traffic. Built-in power management logic and advanced PLL design allows aggressive power state management and optimal system power usage.

At the system level, the LPDDR54 PHY was designed with minimal package substrate layer and PCB layer count in mind. This enables the integration of a LPDDR memory sub-system solution in cost sensitive applications, such as consumer edge devices, digital set-top-box and TV, SSD controllers, and application processors.



LPDDR54 PHY

Key Features

DRAM supports

- *JESD209-5A(LPDDR5), JESD209-4C(LPDDR4), JESD209-4-1(LPDDR4X) compliant*
- *Operating speed up to 6400Mbps in LPDDR5, 4266Mbps in LPDDR4(X)*
- *Multiple DFICLK:CK:WCK ratios*

High Performance

- *Channel equalization with FFE and DFE*
- *Voltage and temperature drift compensation to maintain optimal data eye*

DFT Features

- *Internal and external loopback through datapath*
- *IO bypass mode for internal clock observation*
- *Analog test ports for internal analog signals observation*

Special Features

- *Firmware-based PHY independent initialization of DRAM and training*

Benefits

Power Advantage

- *Supports multiple frequency states with fast switching time*
- *Multiple power saving states with various exit times*
- *Supports DFI frequency ratios of 1:2 and 1:4*

Ultra Low Latency

- *Ultra low read/write latency with programmable PHY boundary timing*

Low Implementation BOM Cost

- *Support low cost 2-2-2 package substrate*
- *Designed for 6-layer PCB as the minimum layer count*

Performance and Power Tuning

- *Software included for performance and power tuning on customer platform*

Deliverables

- **PHY Databook**
- **Implementation Guideline**
- **Package and PCB Design Guideline**
- **Test and Characterization Guideline**

- **Hard-IP Layout (GDS II)**
- **Hard-IP Layout Abstract (LEF)**
- **Hard-IP Liberty Timing Models (.lib)**
- **Hard-IP LVS Netlist (CDL)**
- **IO IBIS models**

- **Verilog Behavior Models and RTL**
- **Example Test Benches**
- **Synthesis and STA Constraints**
- **Physical Verification Reports**